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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/020,407	12/12/2001	Robert Madge	01-299 71739	8733

24319 7590 11/15/2002

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EXAMINER
COTHORN, JUDITH A

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 11/15/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/020,407	Applicant(s) MADGE ET AL.
	Examiner Judith A. Cothorn	Art Unit 2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 8-10* is/are rejected.

7)☒ Claim(s) *5-7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This office action is in response to the filing of the application on 12/12/01.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 - 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thibeault, C., ("On the Comparison of IDDQ and IDDQ Testing", VLSI Test Symposium, 1999, Proceedings. 17th IEEE, pp.143-150) as applied to claim 1, and further in view of Sabade et al. ("Improved wafer-level spatial analysis for IDDQ limit setting", Test Conference, 2001, Proceedings. International, pp. 82-91).

Thibeault discloses a method comprising the steps of: measuring quiescent current of chip to chip or wafer to wafer vectors (column 2, lines 22-29); calculating a difference between a value of the selected parameter at a target location and that of an identical relative location with respect to the target location for each of the plurality of electronic circuits to generate a distribution of differences (column 3, lines 9-16); calculating an absolute value of the distribution of differences (figure 1; column 3, line 38 – column 4, line 4); and calculating an average of the absolute value of the distribution of differences to generate a representative value for the residual for the identical relative location (figure 5).

Thibeault fails to disclose the measuring of quiescent current in neighboring die or plotting the residual as a function of the identical relative location to determine a spatial correlation pattern of the selected parameter.

Sabade et al. disclose the measuring of quiescent current in neighboring die (page 83-page 84) plotting the residual as a function of the identical relative location to determine a spatial correlation pattern of the selected parameter (Figures 4 and 5).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Thibeault to measure the quiescent current of neighboring die as taught by Sabade et al. in order to estimate the process gradient in local wafer regions. It also would have been obvious to plot the residual to determine a spatial correlation pattern in order to show the quiescent current projections on the XY plane of the wafer.

Claims 8, 9, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thibeault, C., ("On the Comparison of IDDQ and IDDQ Testing", VLSI Test Symposium, 1999, Proceedings. 17th IEEE, pp.143-150) as applied to claim 1, and further in view of Sabade et al. ("Improved wafer-level spatial analysis for IDDQ limit setting", Test Conference, 2001, Proceedings. International, pp. 82-91).

Thibeault discloses a method comprising the steps of: measuring quiescent current of chip to chip or wafer to wafer vectors (column 2, lines 22-29); calculating a difference between a value of the selected parameter at a target location and that of an identical relative location with respect to the target location for each of the plurality of electronic circuits to generate a distribution of differences (column 3, lines 9-16); calculating an absolute value of the distribution of differences (figure 1; column 3, line 38 – column 4, line 4); and calculating an

average of the absolute value of the distribution of differences to generate a representative value for the residual for the identical relative location (figure 5).

Thibeault fails to disclose the measuring of quiescent current in neighboring die or plotting the residual as a function of the identical relative location to determine a spatial correlation pattern of the selected parameter. Thibeault also fails to disclose the rejection of any of the plural integrated circuit die having a quiescent current value outside the expected value range.

Sabade et al. disclose the measuring of quiescent current in neighboring die (page 83-page 84) plotting the residual as a function of the identical relative location to determine a spatial correlation pattern of the selected parameter (Figures 4 and 5). Sabade et al. also disclose the rejection of any of the plural integrated circuit die having a quiescent current value outside the expected value range (page 85, elimination of gross outliers).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Thibeault to measure the quiescent current of neighboring die as taught by Sabade et al. in order to estimate the process gradient in local wafer regions. It also would have been obvious to plot the residual to determine a spatial correlation pattern in order to show the quiescent current projections on the XY plane of the wafer. Additionally, it would have been obvious to reject any of the plural of integrated circuit die having a quiescent current value outside the expected value range in order to eliminate obtain a good estimate of fault free IDDQ and to eliminate maverick lots.

Allowable Subject Matter

Claims 5-7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The additionally cited art disclose information on IDDQ testing.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Judith A. Cothorn whose telephone number is 703-305-4733. The examiner can normally be reached on Mon-Fri, 8am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 703-308-4905. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

jac
November 1, 2002

Mary Wilczewski
Primary Examiner